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10/024,065	12/18/2001	Hisashi Nagata	56800 (46547)	5285

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EXAMINER	
LEWIS, DAVID LEE	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/024,065	Applicant(s) NAGATA ET AL.	
	Examiner David L Lewis	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 8, 10-13, and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Ino et al. (6242328 B1).

2. **As in claims 1 and 8, Ino et al. teaches** of a display device comprising: an active matrix substrate, column 3 lines 11-25; a counter electrode, column 3 lines 1125; a display medium layer interposed between the active matrix substrate and the counter electrode, column 3 lines 11-25; and a plurality of pixels, column 3 lines 1125, wherein the active matrix substrate includes: a base plate, figure 7A item 41; a plurality of pixel electrodes formed on the base plate, figure 2 item 20, each said pixel electrode being associated with one of the plurality of pixels, column 6 lines 35-60; a plurality of pixel switching elements, each said pixel switching element being connected to associated one of the pixel electrodes, figure 2 item 21; a plurality of gate lines for controlling operations of the pixel switching elements, figure 2 item 11; a plurality of data lines, each said data line being connected to associated ones of the pixel electrodes by way of associated ones of the pixel switching elements so as to supply a data signal there through, figure 2 item 12; a plurality of data line switching elements, figure 15 item 66, each said data line switching element having terminals, one of said terminals being connected to associated one of the data lines, figure 15 item Qn; a plurality of signal input terminals, each said signal input terminal being connected to another terminal of associated one of the data line switching elements and another terminal of another associated one of the data line switching elements, figure 15 item Qn+1, column 9 lines 45-65, column 10 lines 20-25; a data line branching section, which is provided between the signal input terminals and the data line switching elements, figure 15 item Q; and a control line, which is connected to the data line switching elements to selectively turn ON or OFF the data line switching elements, figure 15 item 68, wherein a signal to turn ON the data line switching elements and a signal to turn ON the pixel switching elements

have mutually different polarities, figure 16 items Q(n), SL1-3, and Vg, column 11 lines 1-30. Wherein said mutually different polarities are inherent to the switching structure taught by Ino. The mutuality is governed by the switch control circuit 68 and the different polarities are governed by the image data output at Q(n) for each color which combines to form a pixel image.

3. **As in claim 10, Ino et al. teaches** of an active matrix substrate comprising: a base plate, figure 7A item 41; a plurality of pixel electrodes formed on the base plate, column 3 lines 11-24, figure 2 item 20; a plurality of pixel switching elements, each said pixel switching element being connected to associated one of the pixel electrodes, figure 2 item 21; a plurality of gate lines for controlling operations of the pixel switching elements, figure 2 item 11; a plurality of data lines, each said data line being connected to associated ones of the pixel electrodes by way of associated ones of the pixel switching elements so as to supply a data signal there through, figure 2 item 12; a plurality of data line switching elements, each said data line switching element having terminals, one of said terminals being connected to associated one of the data lines, figure 15 item 66; a plurality of signal input terminals, each said signal input terminal being connected to another terminal of associated one of the data line switching elements and another terminal of another associated one of the data line switching elements, figuere 15 item Q(n); a data line branching section, which is provided between the signal input terminals and the data line switching elements, figure 15 item Q; and a control line, which is connected to the data line switching elements to selectively turn ON or OFF the data line switching elements, figure 15 item 68, wherein a signal to turn ON the data line switching elements and a signal to turn ON the pixel switching elements have mutually different polarities, figure 16 items Q(n), SL1-3, and Vg, column 11 lines 1-30. Wherein said mutually different polarities are inherent to the switching structure taught by Ino. The mutuality is governed by the switch control circuit 68 and the different polarities are governed by the image data output at Q(n) for each color which combines to form a pixel image.

4. **As in claim 11, Ino et al. teaches** of a display device comprising a display region unit, wherein the display region unit includes: a substrate on which a plurality of pixels are arranged in columns and rows, column 3 lines 11-24; a driver for driving the pixels, column 3 lines 20-25; and switching means, formed on the substrate, for changing an electrical connection state between the pixels and the driver, figure 15 item 66, and wherein the switching means includes: a first switching element located closer to one of the pixels, figure 15 item 66Rn; and a second switching element located closer to the driver, figure 66Gn, and wherein a signal to turn ON the first switching element , figure 16 item SL1, and a signal to turn ON the second switching element have mutually different polarities, figure 16 item SL2, column 11 lines 1-30. Wherein said mutually different polarities are inherent to the switching structure taught by Ino. The mutuality is governed by the switch control circuit 68 and the different polarities are governed

by the image data output at Q(n) for each color which combines to form a pixel image.

5. **As in claim 12, Ino et al. teaches** of a method for driving a display device, the display device comprising: an active matrix substrate, figure 7A item 41; a counter substrate, which is disposed so as to face the active matrix substrate and includes a counter electrode, column 3 lines 11-24; and a display medium layer interposed between the active matrix and counter substrates, column 3 lines 11-24, wherein the active matrix substrate includes: a base plate, figure 7A item 41; a plurality of pixel electrodes formed on the base plate, column 3 lines 11-24, figure 2 item 20; a plurality of pixel switching elements, each said pixel switching element being connected to associated one of the pixel electrodes, figure 2 item 21; a plurality of gate lines for controlling operations of the pixel switching elements, figure 2 item 11; a plurality of data lines, each said data line being connected to associated ones of the pixel electrodes by way of associated ones of the pixel switching elements so as to supply a data signal there through, figure 2 item 12; a plurality of data line switching elements, each said data line switching element having terminals, one of said terminals being connected to associated one of the data lines, figure 15 item Q(n); a plurality of signal input terminals, each said signal input terminal being connected. to another terminal of associated one of the data line switching elements and another terminal of another associated one of the data line switching elements, figure 15 item Q(n+1); a data line branching section, which is provided between the signal input terminals and the data line switching elements, figure 15 item Q; and a control line, which is connected to the data line switching elements to selectively turn ON or OFF the data line switching elements, figure 15 item 68, wherein a signal to turn ON the data line switching elements and a signal to turn ON the pixel switching elements have mutually different polarities, figure 16 items Q(n), SL1-3, and Vg, and wherein the method drives the display device in such a manner that an interval, in which one of the pixel switching elements is turned OFF to hold a potential level of associated one of the data lines as applied to associated one of the pixel electrodes, overlaps at least partially with an interval, in which one of the data line switching elements that is associated with the data line is turned OFF to hold a potential level of the data signal on the data line, for the pixel electrode and the counter electrode that face each other via the display medium layer, figure 16 items Q(n), SL1-3, and Vg, column 11 lines 1-30. Wherein said mutually different polarities are inherent to the switching structure taught by Ino. The mutuality is governed by the switch control circuit 68 and the different polarities are governed by the image data output at Q(n) for each color which combines to form a pixel image.

6. **As in claims 13 and 19, Ino et al. teaches** of a display device comprising: a pair of substrates that: is disposed so as to face each other and be spaced apart from each other, column 3 lines 11-24; a display medium layer interposed between the pair of substrates, column 3 lines 5-24; and a plurality of pixels,

wherein a plurality of counter signal electrodes, each of which extends in a column direction and through which a data signal is supplied, are formed on one of the pair of substrates, column 3 lines 11-24, and wherein the other of the pair of substrate includes: a plurality of pixel electrodes arranged in matrix, figure 2 item 20, each said pixel electrode being associated with one of the plurality of pixels, figure 7A items 42, 48, and 49; a plurality of pixel switching elements, each of which is connected to associated one of the pixel electrodes, figure 2 item 21; a plurality of gate lines, which extend in a row direction and are used for controlling operations of the pixel switching elements, figure 2 item 11; and a plurality of common lines, each of which is connected to associated ones of the pixel electrodes by way of associated ones of the pixel switching elements, figure 2 item Vcom, and wherein the display device further includes a plurality of signal electrode switching elements, each of which is connected to associated one of the counter signal electrodes and controls supply of the data signal to the counter signal electrode, figure 15 item 66, and wherein a signal to turn ON the signal electrode switching elements and a signal to turn ON the pixel switching elements have the same polarity, figure 16 items SL1-3 and Vg, column 11 lines 1-30. Wherein said opposite electrode is inherent to the structure of Ino as known in the art and used for the purpose of creating an electric field across the display element altering the display contrast to form an image.

7. **As in claim 20, Ino et al. teaches** of a method for driving a display device, the display device including: a pair of substrates that is disposed so as to face each other and be spaced apart from each other, column 3 lines 11-24; and a display medium layer interposed between the pair of substrates, wherein a plurality of counter signal electrodes, each of which extends in a column direction and through which a data signal is supplied, are formed on one of the pair of substrates, column 3 lines 5-24, figure 7, and wherein the other of the pair of substrates includes: a plurality of pixel electrodes arranged in matrix, figure 2 item 20; a plurality of pixel switching elements, each of which is connected to associated one of the pixel electrodes, figure 2 item 21; a plurality of gate lines, which extend in a row direction and are used for controlling operations of the pixel switching elements, figure 2 item 11; and a plurality of common lines, each of which is connected to associated ones of the pixel electrodes by way of associated ones of the pixel switching elements, figure 2 item Vcom, and wherein the display device further includes a plurality of signal electrode switching elements, each of which is connected to associated one of the counter signal electrodes and controls supply of the data signal to the counter signal electrode, figure 15 item 66, and wherein the method drives the display device in such a manner that an interval, in which one of the pixel switching elements is turned OFF to hold a potential level on associated one of the common lines as applied to associated one of the pixel electrodes, figure 16 item Vg, overlaps at least partially with an interval, in which one of the signal electrode switching elements is turned OFF to hold a potential level of the data signal as applied to associated one of the counter signal electrodes, for the pixel electrode and the counter

signal electrode that face each other via the display medium layer, figure 16 item SL1-3, Vcom, column 11 lines 1-30. Wherein said opposite electrode is inherent to the structure of Ino as known in the art and used for the purpose of creating an electric field across the display element altering the display contrast to form an image.

8. **As in claim 21, Ino et al. teaches** of a display device comprising: a pair of substrates that is disposed so as to face each other and be spaced apart from each other, column 3 lines 11-24; and a display medium layer interposed between the pair of substrates, wherein a plurality of counter signal electrodes, each of which extends in a column direction and through which a data signal is supplied, are formed on one of the pair of substrates, column 3 lines 5-24, and wherein the other substrate of pair of includes: a plurality of pixel electrodes arranged in matrix, figure 2 item 20; a plurality of pixel switching elements, each of which is connected to associated one, of the pixel electrodes, figure 2 item 21; a plurality of gate lines, which extend in a row direction and are used for controlling operations of the pixel switching elements, figure 2 item 11; and a plurality of common limes, each of which is connected to associated ones of the pixel electrodes by way of associated ones of the pixel switching elements, figure 2 item Vcom, and wherein the display device further includes a plurality of signal electrode switching elements, figure 15 item 66, each of which is connected to associated one of the counter signal electrodes and controls supply of the data signal to the counter signal electrode, figure 15 items 64 and 68.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-7, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ino et al. (6424328 B1).

10. **As in cancelled claim 9, Ino et al. teaches** of the an active matrix substrate as applied to remaining independent claims. However Ino et al. is silent as to the combination wherein each said pixel switching element is an n-channel transistor or a p-channel transistor, while each said data line switching element includes an n-channel transistor and a p-channel transistor that are connected in parallel with each other, and wherein in the data line switching element, one of the n and p-

channel transistors that has a polarity different from that of the pixel switching element has a channel length or channel width greater than that of the other transistor. Ino however teaches of analog switches comprised of TFT's having a gate structure shown in figures 7A,B, column 9 line 64 to column 10 line 5, wherein said analog switches are known to be comprised of a single MOS type p-channel and/or single n-channel device, also wherein both p and n channel devices are shown in a parallel configuration. Figures 2 item 21 and figure 3 item 32 of Ino et al. show n-channel switching devices while figure 15 item 66 shows analog switches know to be of said n and p type devices in a parallel configuration. Ichikawa et al. shows such a configuration comprising said parallel configuration, figure 1 item 12-17, wherein the data line switching elements are of the known analog switches. Further in figure 9 items 323 and 324, Ichikawa et al. shows the switching devices a the p or n type device, and wherein any drive scheme of the nMos transistor type is capable of configurement in the pMos transistor type, column 8 lines 45-60, further wherein one of the n and p-channel transistors that has a polarity different from that of the pixel switching element has a channel length or channel width greater than that of the other transistor, column 7 lines 54-67. Therefore the motivation to combine Ino and Ichikawa lies in the fact that Ichikawa suggests know implementations to providing for analog switches and alternative pixel switching transistors of the n or p type having a channel length or width ratio as claimed, in the liquid crystal display apparatus taught by Ino et al., which would have been obvious to the skilled artisan at the time of the invention given said motivation, and the fact that teaches teach of like TFT active matrix driven pixel display systems with data line and pixel switching elements as claimed.

11. **As in claims 2-6 and 15-18**, the same reasons of obviousness ass applied above to cancelled claim 9, further Ino in view of Ichikawa teaches of said channel width relationships, column 7 lines 50-67, both n and p transsitor variations, column 8 lines 50-60, said parallel n and p transistor, figure 1 item 12, said n and p pixel transistors, figure 9 items 323 and 324, column 13 lines 5-15. **As in claim 7**, Ino in view of Ichikawa teaches of wherein each said pixel switching element and each said data line switching element both have a semiconductor layer, which has been deposited on the base plate, as a transistor active region, column 13 lines 10-25, Ino, column 6 lines 25-40. **As in claim 14**, Ino in view of Ichikawa teaches of wherein the signal electrode switching elements and the pixel switching elements are formed on the same substrate, column 6 lines 25-40, and includes signal electrode transfer sections, figure 4 item 12.

Response to Arguments

12. Applicant's arguments filed 4/19/2004 have been fully considered but they are not persuasive. **Applicant argues** there is no discussion anywhere in Ino regarding Q(n) that discloses or describes that the signals being applied to the data lines switching elements and the pixel switching elements to turn these switching elements ON have mutually different polarities. The Examiner disagrees because said mutually different polarities are inherent to the switching structure taught by Ino. The mutuality is governed by the switch control circuit 68 and the different polarities are governed by the image data output at Q(n) for each color which combines to form a pixel image. **Applicant argues** that the Ino fails to teach of an opposite electrode. The Examiner disagrees because said opposite electrode is inherent to the structure of Ino as known in the art and used for the purpose of creating an electric field across the display element altering the display contrast to form an image. **Applicant argues** the said respective OFF conditions cannot overlap. The Examiner disagrees because figure 16 shows an overlap of signals SL1-3 and Vcom within one horizontal scanning period. **Further** the motivation to combine Ino and Ichikawa lies in the fact that Ichikawa suggests known implementations to providing for analog switches and alternative pixel switching transistors of the n or p type having a channel length or width ratio as claimed.

Conclusion

13. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L Lewis whose telephone number is 703 306-3026. The examiner can normally be reached on M, T, TH, F. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-4700.

Any response to this action should be mailed to:
Commissioner of Patents and Trademarks
Washington, D.C. 20231
or faxed to:
(703) 872-9314 (for Technology Center 2600 only)
Hand-delivered responses should be brought to
Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600